Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-9. (Canceled)

10. (Previously Presented) A liquid crystal device, comprising:

plural data lines;

plural scanning lines intersecting the data lines;

plural pixels provided in an array inside an image display area, by corresponding to intersections of respective data lines and scanning lines; and

a driver section which supplies image signals to the pixels,

wherein the driver section comprises a data driver which supplies an image signal for which a potential is inverted into a positive polarity potential or a negative polarity potential for each one horizontal period, to each of said plural data lines, and a scanning driver which sequentially shifts a gate-output pulse in synchrony with a clock signal which rises for each one horizontal period, and

n ($n \geq 2$) gate-output pulses are supplied to the scanning driver at a different timing within one vertical period in a picture signal,

the scanning driver shifts each of the n gate-output pulses in synchrony with the clock signals, and also supplies a scanning signal to each scanning line, based on each of alternately rising m enable signals and each of the n gate pulses.

11. (Previously Presented) The liquid crystal device according to claim 10, wherein;

the n gate-output pulses are two gate-output pulses,

the two gate-output pulses are supplied to the scanning driver with a time lag of 1/2 of a vertical period in the image signal each other,

the scanning driver outputs two scanning signals alternately based on each of the two gate-output pulses and each of first and second two alternately rising enable signals

each of the two scanning signals is supplied to each of two scanning lines, and

a distance between the two scanning lines is corresponding to 1/2 of the image display area.

12. (Previously Presented) The liquid crystal device according to claim 10, wherein the four gate-output pulses are supplied to the scanning driver with a time lag of 1/4 of a vertical period in the image signal each other,

the scanning driver outputs four scanning signals alternately based on each of the four gate-output pulses and each of first through fourth four alternately rising enable signals

each of the four scanning signals is supplied to each of four scanning lines, and

a distance between each of the four scanning lines is corresponding to 1/4 of the image display area.

13. (Canceled)

14. (Original) The liquid crystal device according to claim 10, wherein a memory is provided in said driver section,

while an image signal input from the outside is being supplied to said data driver, the image signal is also stored in said memory, and

said data driver alternately supplies in each of the one horizontal periods, an image signal input from the outside, and image data read out from said memory, and also inverts the polarity of the image data read out from said memory with respect to said image signal, to thereby supply an image signal for which the polarity is inverted into the positive polarity potential or the negative polarity potential for each one horizontal period, to each of said plural data lines.

15-22. (Canceled)

23. (Previously Presented) A drive method for a liquid crystal device that includes plural data lines, plural scanning lines intersecting the data lines, plural pixels provided in an array inside an image display area, by corresponding to intersections of respective data lines and scanning lines, and a driver section which supplies image signals to the pixels, the method comprising:

supplying, with a data driver of the driver section, an image signal for which a potential is inverted into a positive polarity potential or a negative polarity potential for each one horizontal period, to each of the plural data lines;

sequentially shifting, with a scanning driver of the driver section, a gate-output pulse in synchrony with a clock signal which rises for each one horizontal period;

supplying ($n \geq 2$) gate-output pulses to the scanning driver at a different timing within one vertical period in a picture signal;

shifting, with the scanning driver, each of the n gate-output pulses in synchrony with the clock signals; and

supplying, with the scanning driver, a scanning signal to each scanning line, based on each of alternatively rising m enable signals and each of the n gate pulses.

24. (Canceled)